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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/511,630	10/19/2004	Takanori Shimizu	NE297-PCT (US)	4085

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MCGINN INTELLECTUAL PROPERTY LAW GROUP, PLLC
8321 OLD COURTHOUSE ROAD
SUITE 200
VIENNA, VA 22182-3817

EXAMINER	
CHIEM, DINH D	
ART UNIT	**PAPER NUMBER**
2883	

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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/511,630	SHIMIZU ET AL.	
	Examiner	Art Unit	
	ERIN D. CHIEM	2883	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *13 November 2007*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1,5,6,8-12,15,16,18 and 21-24* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,5,6,8-12,15,16,18 and 21-24* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1, 4-9, 12-14, and 17-23 are rejected under 35 U.S.C. 103(a) as being unpatentable over Uchida (US 6,897,430 B2).

In terms of claims 1, 12, and 21-23 Uchida discloses an optoelectronic hybrid integrated module (Fig. 3) and a logic LSI (Fig. 4, 1103) wherein the optoelectronic hybrid integrated module includes: an optical device for converting one Of an optical signal into an electric signal and an electrical signal and an electrical signal into an optical signal (col. 3, lines 4-9 and col. 6, line 59 to col. 7 line 17); an input/output IC for drive-controlling the optical device (1201, 1208); and a transparent base material having electric wiring and light permeability (1205 upper clad; 1206 core; 1207 lower clad); wherein the optical device and the input/output IC are flip-chip mounted (1202) on a surface of the transparent base material; and wherein the electric wiring connects the optical device and the input/output IC so as to transfer an electric signal between them, and the electric wiring being positioned on a surface of the transparent base material (1104) opposite the surface where the optical device is mounted (since the optical device 1203, 1208) are spherical and are partially mounted within the substrate, examiner considers the electric wiring 1104 to be on the opposite surface of where the optical device is mounted), the

electric wiring being provided as a ground electrode and serving as an electromagnetic shield for the optical device and the input/output IC (col. 13, lines 24-30). Furthermore, the logic LSI controls an electric signal input into or output from the optoelectronic hybrid integrated module (col. 12, lines 48-49), and wherein the optoelectronic hybrid integrated module and the logic LSI are mounted on the same substrate (Please see Fig. 3 and 4 for detail). The grounds of rejection reference Fig 3 and 4. A more detailed blown up view of the elements are also show in Figure 30 which better illustrates the wiring and interaction of each element to each other wherein "the optical device [4109 and 4106] and the input/output IC [4102] are flip-chip mounted on a surface [4105 and 4103] of the transparent base material [4108 and 4107] substantially aligned with the light couple means [4104]". Further newly amended limitations wherein the optical device and IC flip-chip mounted on a surface of the transparent material substantially aligned with the light couple means is also disclosed in Figure 30 to the prior art of Uchida.

However, Uchida does not teach the light emitting device is mounted on the transparent base material. It would have been obvious to one having ordinary skill in the art at the time the invention was made to mount the light-emitting device on the transparent base material dependent on the device specification, since it has been held that constructing a formerly integral structure in various elements involves only routine skill in the art. Nerwin V. Erlichman, 168 USPQ 177, 179. Examiner welcomes the applicant to contend to examiner's argument by presenting unexpected result from experimentation that would show the advantage of a mounted light-emitting device as claimed.

Regarding claims 5-9, 13-14, and 17-20, Uchida discloses element 1208 is a light emitting device which converts an electric signal into an optical signal and outputs it (1211), and

the input/output IC comprises a driver IC which outputs an electric signal to the optical device (col. 12, lines 39-42). Incorporated within the module is a light receiving device, which converts an optical signal into an electric signal (1203), and the input/output IC comprises an electric amplifier IC that amplifies an electric signal from the light-receiving device (col. 3, lines 34-36). Uchida further discloses the transparent base material comprises a transparent plate transmitting a light and the transparent plate (1205, 1206, 1207) comprises a material having high permeability to a wavelength of the optical device. The transparent base material comprises a flexible sheet transmitting a light, and the flexible sheet comprises a material having high permeability to a wavelength of the optical device (col. 3, lines 60-62). The optical device is further positioned directly under the light inputting/outputting portion (Fig. 7, '1706' '1780'). Applicant has not defined the scope of the material having "high permeability to a wavelength of the optical device" thus Uchida references reads upon the limitation since light is traveling through layer 1206, therefore, Uchida flexible transparent substrate has a high permeability to a wavelength of the optical device. Uchida teaches the means for light coupling are the embedded optical devices 1203 and 1208 that is integrally formed with the transparent base material.

Regarding claim 9, notice in Fig. 4 that the light receiver and light transmitter also acts as an axis converter wherein the light axis is changed and referenced by the directionality of the arrows (1203, 1208).

Regarding claim 18, the light inputting/outputting portion comprises a convex lens formed on the transparent base material is shown in Fig. 4. Examiner considers the spherical lens protruding above the substrate (1104) to be the convex lens. And elements 1203 and 1208 optical receiver/transmitter are coupling units; coupling light into or out of the unit as obviated by the

aforementioned terms (1210, 1211).

Claims 10-11, and 15-16 are rejected under 35 U.S.C. 103(a) as being unpatentable over Uchida. Uchida discloses the invention of claim 1; however Uchida does not discloses the device and the input/output IC comprise an interpose which comprises a holder, a heat spreader, the transparent base material is fixed to a holding frame within which electric wiring is incorporated, and the optical device is sealed to the transparent base material devoid of an air gap.

Verdiell discloses an optoelectronic assembly which comprises of an interpose which further comprises a holder (fig. 1; '20'), a heat spreader (20) Verdiell calls '20' a raised platform (Para [00207]). Examiner also considers this "raised platform" as a holding frame within which electric wiring is incorporated (Para [0027]). Furthermore, Verdiell discusses a key property of the optoelectronic package is hermetic, wherein the components within the housing is filled through vias such that the sealed package is devoid of air gap (Para [0033]-[0037]).

Since Uchida and Verdiell are both from the same field of endeavor, the purpose disclosed by Verdiell would have been recognized in the pertinent art of Uchida.
It would have been obvious at the time the invention was made to a person having ordinary skill in the art to recognize the teaching of Verdiell of packaging the optoelectronic device for end-user handling and installation. The motivation for incorporating Verdiell teaching to Uchida's optoelectronic device is to encompass electrical and optical component of the a module within an encasing housing that prevents the electrical components from being damaged by environmental exposure.

Regarding claim 24, Uchida teaches the device of Claim1, wherein the light coupling means improves light coupling efficiency. The examiner consider this to be a functional require

of which is perform by the coupling means [4104]. Since this structure is capable of coupling light therefore the coupling efficiency between the IC and optical waveguide are enhance by this structure.

Response to Arguments

Applicant's arguments filed 11/13/2007 have been fully considered but they are not persuasive.

In this instant the applicant argues that the prior art to Uchida does not teach "the optical device and the input/output IC are flip-chip mounted on a surface of the transparent base material substantially aligned with the light couple means". The examiner respectfully disagrees for the following reason(s):

The grounds of rejection reference Fig 3 and 4. A more detailed blown up view of the elements are also show in Figure 30 which better illustrates the wiring and interaction of each element to each other wherein "the optical device [4109 and 4106] and the input/output IC [4102] are flip-chip mounted on a surface [4105 and 4103] of the transparent base material [4108 and 4107] substantially aligned with the light couple means [4104]". Further newly amended limitations wherein the optical device and IC flip-chip mounted on a surface of the transparent material substantially aligned with the light couple means is also disclosed in Figure 30 to the prior art of Uchida.

For the reason above the grounds of rejection are maintained.

Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL.** See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to ERIN D. CHIEM whose telephone number is (571)272-3102. The examiner can normally be reached on Monday - Thursday 9AM - 5PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Frank G. Font can be reached on (571) 272-2415. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Erin D Chiem/

Examiner, Art Unit 2883

Frank G. Font
Supervisory Patent Examiner
Technology Center 2800